REMARKS/ARGUMENTS

In light of the above amendments and remarks to follow, reconsideration and allowance of this application are respectfully requested.

Claims 1-9, 11 and 13 are pending in this application. Claims 10 and 12 are canceled. Please note claims 10-13 were newly presented in the previous amendment, but not acknowledged by the Examiner.

The title was objected to as not being descriptive. Applicants have amended the title to clearly indicate the invention to which the claims are directed. Accordingly, Applicants believe this objection has been overcome.

Claims 1-2 and 5-6 were rejected under 35 U.S.C. §102(e) as being anticipated by Kojima (U.S. Patent 6,944,801).

In the present invention of claim 1, a plurality of configuration information stored in a plurality of registers is selectively switched by a switching means to configure a delay means. (Figure 1; elements 145, 146, and 142) A delay element array in the delay means is configured based on the configuration information. (Specification paragraph 14) This feature of the present invention allows the characteristics of the delay means to be adjusted to the same characteristics as those of the critical path of the target circuit.

First, Kojima does not disclose or suggest the recited configuration information. The Examiner insists that Kojima's managing CPU 300 produces configuration information which is sent to the delay means [from the output of 140]. According to Kojima, managing CPU 300 generates a setup signal 110 which is sent to selector value register 140 which then chooses selectors

from amongst selectors 150 through 150N based on the setup signal 110. Therefore, the setup signal 110 is the signal that determines delay gates in the delay circuit. (See Kojima column 4, lines 50-53). However, the setup signal 110 does not indicate "the number of stages of element arrays to fabricate the delay characteristics of a critical path of said target circuit" as recited in the present claims. (Claims 1 and 5)

Rather, Kojima compares the bit values between write data holding register 170 and read data buffer 180. (Column 7, lines 7-9) If they don't match, the value of variable i, which is set to the selector value setting register 140, is incremented by 1 and the output of the delay gate on the immediately preceding stage is selected by the selector. (Column 7, lines 23-26) This routine (from step S102 to S107) is repeated until the skew adjustment is completed (i.e. the bit values are matched) or the variable i exceeds (M+1). (Column 7, lines 23-26)

In contrast, the present invention's configuration information indicates the number of stages of element arrays to fabricate the delay characteristics of a critical path of a target circuit. This feature allows the characteristics of the delay means to be adjusted to the same characteristics as those of the critical path of the target circuit but without repeating any steps. Moreover, Kojima mentions that when the variable i is equal to or greater than (M+1) at step S106, skew of the output of the data flip flop, which should be adjusted, cannot be fixed and the device ends its process. (Column 7, lines 15-19) On the other hand, the present invention guarantees to fix the characteristics of the delay means to the same characteristics as those of the critical path of the target circuit.

Second, Kojima fails to disclose or suggest the plurality of registers for setting therein a plurality of

configuration information for forming said delay element arrays. The Examiner insists that Kojima's write data holding registers 170 and 270 have the same function. However, Kojima discloses the write data holding registers hold the output data of the data flip flops 131, 132,..., and 13N. Then the data is simply sent to managing CPU 300. (Column 4, lines 54-57) This means that Kojima fails to disclose the write data holding registers 170 and 270 store a plurality of configuration information.

In contrast, the present invention possesses a distinctly different function. A plurality of registers (145 in Fig. 1) can store a plurality of configuration information, as mentioned above. By referring to this configuration information set in the register group, the characteristics of the delay means is adjusted to correspond with the critical path of the target circuit without repeating any steps.

Wherefore, Kojima fails to anticipate the present invention and the rejected claims should now be allowed.

Applicant appreciates the Examiner's acknowledgment that claims 3-4 and 7-9 would be allowable if rewritten in independent form. However, for the reasons discussed above, Applicant has decided not to amend these claims at this time.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

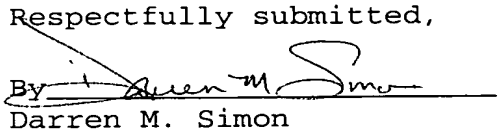
If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's

attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095.

Dated: February 13, 2007

Respectfully submitted,

By 

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